REMARKS

Claims 1-16 are presently pending. Reconsideration is respectfully requested in view of the following remarks.

Claim 1 was rejected under 35 U.S.C. § 103(a) as being obvious from the combination of Rana and Agarwal. Final Office Action at 2. Claim 1 recites, among other limitations, "the contents of the memory location associated with the address received from the code address bus being incremented responsive to receipt of the address".

Examiner has indicated that "Rana does not teach the contents of the memory location associated with the address received form the code address bus being incremented responsive to the receipt of the address, however, Rana does teach the code coverage memory storing code coverage data of predetermined bit patterns that includes hexadecimal value "00" and changed to value "ff" to determine if the code has been executed (See Col. 8, lines 31-44). Agarwal discloses code coverage testing and flagging code that has been executed. In addition to just flagging the code that has been executed, Agarwal also teaches incrementing a value of the associated memory (see Agarwal, paragraphs 0123, 0124, and 0127). It would have been obvious to one or ordinary skill in the art at the time of the invention to combine the user of a predetermined bit pattern of the executed code or Rana with the storing of an incremented value associated with execute code of Agarwal. This would have been obvious to one or ordinary skill in he art at the time of the invention nto dobecause it allows for keeping count of the number of times the code has been executed (See Agarwal, paragraph 0124)." OA at 3.

Examiner also notes that "Rana uses one known value to indicate code that has not been executed and one known value to indicate code that has been executed. Agarwal allows for indicating that code has been executed and also how many times it has been executed. The use of the incremented value does not render the predetermined value unsatisfactory for its purpose, but rather enhances it. Therefore a first 'predetermined' value is used to indicate the code has not been executed and additional 'predetermined' values are used to indicate the code has been executed along with additional information indicating the number times it has been executed." Office Action at 11-12.

Assignee respectfully traverses. Rana teaches "hexadecimal 'ff' may be loaded from the register 58 to the code coverage memory 10 in one test, and hexadecimal '00' may be loaded in another test." Assignee first takes exception to Examiner's assertion that "Rana uses one known value to indicate code that has not been executed". Note that neither 'ff' or '00' are used as "a value to indicated code that has not been executed". Rather "'ff' may be loaded from the register 58 to the code coverage memory 10 **in one test**, and hexadecimal '00' may be loaded in **another test.**" Given that one known value, 'ff', is used for one test, and another value '00' is used in another test, incrementing these values would result in ambiguity. For example, '01' could either mean that the test corresponding to '00' was executed once or that the test corresponding to 'ff' was executed twice, '02' could either mean that the test corresponding to '00' was executed twice or that the test corresponding to 'ff' was executed three times. Accordingly, modifying Rana with Agarwal, as proposed by

Examiner would render Rana unsuitable for its intended purpose.

Accordingly, Assignee respectfully traverses the rejection of claims 1 and 9 and requests that Examiner withdraw them.

Claim 2 was rejected under 35 U.S.C. § 103(a) as being obvious from the combination of Rana and Agarwal. Claim 2 recites, among other limitations, "an address multiplexer for making a first selection between the input and an address counter, and for providing the first selection to the memory", where "the input" takes antecedent basis from "an input for receiving an address from a code address bus".

Examiner has indicated that "Rana teaches the address lines of the emulation circuit being multiplexed (See Rana, Col. 10 lines 63-64)." Office Action at 12. Assignee respectfully traverses and notes that Rana, Col. 10, Lines 63-64 merely teaches "Port 0: data and address lines 48 of the emulation circuit 40 (multiplexed);". The foregoing does not teach or fairly suggest "an address multiplexer for making a first selection between the input and an address counter, and for providing the first selection to the memory". Accordingly, Assignee respectfully traverse the rejection to claims 2 and 10 and requests that Examiner withdraw it.

Regarding claim 15, Examiner objected to the claim indicating that "Claim 15 cites both inputs of the multiplexer being the first selection." Assignee respectfully traverses and notes that "the first selection" claims antecedent basis "a first selection" in claim 2. The circuit of claim 14, wherein

In claim 15, “if the input for receiving an address from a code address bus is the first selection”, the “multiplexer directly connects the first input to the output” and “if the address counter is the first selection”, the multiplexer “directly connects the second input to the output”.

CONCLUSION

For at least the foregoing reasons, Assignee respectfully submits that each of the pending claims are allowable and Examiner is respectfully requested to pass this case to issuance. The Commissioner is hereby authorized to charge additional fees or credit overpayments to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

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Respectfully submitted,

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